Compensation of Voltage Harmonics and Unbalance in Micro grids using Secondary Control Technique

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Abstract- In this paper, a hierarchical control scheme is proposed for enhancement of Sensitive Load Bus (SLB) voltage quality in micro grids. The control structure consists of primary and secondary levels. The primary control level comprises Distributed Generators (DGs) local controllers. Each of these controllers includes a selective virtual impedance loop which is considered to improve sharing of fundamental and harmonic components of load current among the DG units. The sharing improvement is provided at the expense of increasing voltage unbalance and harmonic distortion. Thus, the secondary control level is applied to manage the compensation of SLB voltage unbalance and harmonics by sending proper control signals to the primary level. DGs compensation efforts are controlled locally at the primary level. The system design procedure for selecting proper control parameters is discussed. Simulation results are provided in order to demonstrate the effectiveness of the proposed control scheme.

Index Terms- Distributed Generator (DG), micro grid, voltage harmonics, voltage unbalance, sag, UPQC, statcom, DVR

I. INTRODUCTION

Distributed Generators (DGs) are often connected to the utility grid or micro grid through a power-electronic interface converter. Micro grid is a local grid consisting of DGs, energy storage systems and dispersed loads which may operate in grid-connected or islanded mode [1].

Recently, some control approaches are proposed to control the DG interface converter aiming to compensate power quality problems. A single-phase DG which injects harmonic current to compensate voltage harmonics is presented in [2]. However, in the case of sever harmonic distortion, a large amount of the interface converter capacity is used for compensation and it may interfere with the power supply by the DG. Harmonic compensation approaches of [3]-[5] are based on making the DG units of a power distribution system emulate a resistance at harmonic frequencies. Moreover, a method for compensation of voltage harmonics in an islanded micro grid has been presented in [6]. This method is also based on the resistance emulation and applies a harmonic power droop characteristic in order to share the compensation effort among DGs. The approach presented in [7] is based on controlling each DG unit of a micro grid as a negative sequence conductance to compensate voltage unbalance. The conductance reference is determined by applying a droop characteristic which uses negative sequence reactive power to provide the compensation effort sharing. The control system of [7] is implemented in dq (synchronous) reference frame while [8] addresses the voltage unbalance compensation using _ (stationary) frame control.

The control method presented in [9] is based on using a two-inverter interface converter (one connected in shunt and the other in series with the grid) in order to control power flow and also to compensate the voltage unbalance. This two-inverter structure can be unattractive considering the cost and volume of the DG interface converter. In addition, it should be noted that the methods presented in [3]-[8] are designed to enhance voltage quality at the DG terminal while the power quality at the “Sensitive Load Bus (SLB)” is an important concern in micro grids. Furthermore, if the voltage distortion is compensated locally, it may be amplified in the other buses of the electrical system including the SLB. This phenomenon is called “whack-a-mole” in the case of harmonic distortion [10].

As the first step to address these concerns, the authors proposed a hierarchical control scheme for direct compensation of fundamental voltage unbalance at SLB of a micro grid where the unbalance...
was originated from linear unbalanced loads [11]. In the present paper, this scheme is extended considering unbalanced harmonic distortion caused by nonlinear unbalanced loads. In this case, the negative sequence of fundamental component as well as positive and negative sequences of SLB voltage main harmonics should be compensated.

In the applied hierarchical structure, the central secondary control level manages the compensation by sending proper control signals to the primary level. The sharing of compensation effort among the DGs is controlled locally at the primary level. By sharing the compensation effort, the load current will not necessarily be shared properly, especially, in the micro grids which are noticeably asymmetrical in terms of the line impedances and/or loads distribution. Thus, a selective virtual impedance loop is proposed for each DG unit to improve the load sharing.

![Fig. 1. Detailed block diagram of the control system.](image)

II. DG LOCAL CONTROL SYSTEM

The structure of each DG power stage and local controller is shown in Fig. 1. As it can be seen, a feed forward loop may be included to consider small variations of dc link voltage ($V_{dc}$). The local control of DGs is performed in $\alpha\beta$ reference frame. As shown in “DGj local controller” block, the reference of the DG output voltage in $\alpha\beta$ frame ($V_{o\alpha\beta}^*$) is provided by power controllers, virtual impedance loop and compensation effort controller. Then, according to $V_{\alpha\beta}^*$ and the instantaneous measured output voltage ($V_{\alpha\beta}^0$), the reference current ($I_{\alpha\beta}^*$) is generated. On the other hand, LC filter inductor current is measured, transformed to $\alpha\beta$ frame ($i_{L\alpha\beta}$) and controlled by the current controller to provide voltage reference for pulse width modulator (PWM).

A. Fundamental Positive Sequence Powers Controllers

Control of the active and reactive powers is performed assuming a mainly inductive microgrid. The power controllers determine the reference values of DGs output voltage phase angle and amplitude ($\phi^*$ and $E^*$, respectively) considering the operation mode of microgrid, i.e. islanded or grid connected. Design of the power controllers is sufficiently studied literature (e.g., [15],[16]) and will not be discussed.

B. Voltage and Current Controllers

The following proportional-resonant (PR) voltage and current controllers are applied in this paper.
Where $K_p (K_{pi})$ and $K_{ph} (K_{rh})$ are the proportional and $k$th harmonic (including fundamental component as the first harmonic) resonant coefficients of the voltage (current) controller, respectively. $w_{cv}$ and $w_{ci}$ represent voltage and current controllers cut-off frequencies, respectively.

C. Virtual Impedance Loop

The block diagram of the virtual impedance is depicted in Fig.2 where $R_{vr}^{l+}$, $R_{vr}^{l-}$, and $R_{vr}^{h}$ represent the virtual resistance for fundamental positive sequence, fundamental negative sequence and $h$th harmonic (both positive and negative sequences) components of DG output current, respectively. $L_{vr}$ and $w_O$ are respectively the virtual inductance against fundamental positive sequence current and the rated frequency. In order to provide proper control of fundamental positive sequence powers, the microgrid is made more inductive by including $L_{vr}$. However, a small $R_{vr}^{l+}$ is added to damp the system oscillations [15],[17].

![Fig. 2. Block diagram of selective virtual impedance.](image)

D. Compensation Effort Controller

The compensation effort controller manages the sharing of compensation workload among the microgrid DGs. The block diagram DGj of effort controller is shown in Fig.3. As seen, DG unit output current in $\alpha\beta$ frame ($i_{o\alpha\beta}$) is fed to this controller and positive and negative sequences of its $\alpha$-axis fundamental component ($i_{o+\alpha\beta}$ and $i_{o-\alpha\beta}$) and $h$th harmonic component ($i_{o+\alpha\beta}^h$ and $i_{o-\alpha\beta}^h$) are extracted. Then, $i_{o+\alpha\beta}$, $i_{o-\alpha\beta}$, $i_{o+\alpha\beta}^h$ and $i_{o-\alpha\beta}^h$ are applied to calculate current unbalance factor(UF) and harmonic distortion indices of $h$th harmonic positive and negative sequences (HD+ and HD-, respectively). UF, HD+ and HD- are calculated as the ratio of $i_{o+\alpha\beta}$, $i_{o-\alpha\beta}$ and $i_{o+\alpha\beta}^h$ $rms$ values ($i_{o+\alpha\beta}$, $i_{o-\alpha\beta}$ and $i_{o+\alpha\beta}^h$, respectively) to $rms$ value of $i_{o+\alpha\beta}$ ($i_{o+\alpha\beta}$), respectively. Note that using $\beta$-components for
calculation of unbalance and harmonic distortion indices leads to the same results because the magnitude of α- and β-components is equal for both positive and negative sequences of fundamental and harmonic components.

Finally, the references for compensation of fundamental unbalance and hth harmonic positive and negative sequences by DGj(C_{dq,j}^{1+}, C_{dq,j}^{1-}, and C_{dq,j}^{1+}, respectively) are calculated as shown in Fig. 3 where S_{Oj} the rated capacity of and subscript “max” represent the maximum value. By multiplying the ratio DGj of rated capacity S_{Oj} to the total capacity of the microgrid DGs, compensation effort of each DG will be proportional to its rated capacity.

\[ UF_I, HD_{I}^{h+} \text{ and } HD_{I}^{h-} \] can be considered as the indices of compensation effort because as shown in the simulation results, compensation of SLB voltage unbalance and hth harmonic positive and negative sequences is achieved through injecting corresponding current components by the DGs. Thus, the terms \( (UF_{I,\text{MAX}} - UF_I) \) (HD_{I,\text{MAX}}^{h+}-HD_{I}^{h+}) and (HD_{I,\text{MAX}}^{h-}-HD_{I}^{h-}) in Fig. 6 contribute towards sharing of compensation effort. In fact, increase of each component compensation effort leads to the increase of corresponding index. Consequently, \( (UF_{I,\text{MAX}} - UF_I) \) (HD_{I,\text{MAX}}^{h+}-HD_{I}^{h+}) or (HD_{I,\text{MAX}}^{h-}-HD_{I}^{h-}) decrease and it leads to compensation effort decrease. So, inherent negative feedbacks exist in the effort controller. It is assumed that the maximum values of unbalance factor and harmonic distortion indices are unity. This assumption is valid for most of the practical cases; however, larger constants can be used as the maximum values.

![Fig.3. Block diagram of compensation effort controller](image)

III. SECONDARY CONTROLLER

The block diagram of the secondary controller is also shown in Fig. 1. As seen, \( dq \) components of SLB voltage fundamental positive and negative sequences (\( v_{dq}^{1+} \) and \( v_{dq}^{1-} \)) and \( hth \) harmonic positive and negative sequences (\( v_{dq}^{h+} \) and \( v_{dq}^{h-} \)) are used to calculate voltage unbalance factor (\( UF \)) and \( hth \) harmonic positive and negative sequence distortion indices (\( HD^{h+} \) and \( HD^{h-} \), respectively). Calculation block is similar to "HD&UF Calculation" block of Fig. 3. Then, \( UF_I \), \( HD^{h+} \) and \( HD^{h-} \) are compared with the reference values (\( UF_{ref} \), \( HD_{ref}^{h+} \) and \( HD_{ref}^{h-} \), respectively) and the errors are fed to proportional-integral (PI) controllers. Afterwards, the outputs of these controllers are multiplied by \( v_{dq}^{1-} \), \( v_{dq}^{h+} \) and \( v_{dq}^{h-} \) to generate \( C_{dq}^{1-} \), \( C_{dq}^{h+} \) and \( C_{dq}^{h-} \), respectively. If the unbalance factor or any of the harmonic distortion indices are less than the reference value, the respective deadband block prevents the increase of the distortion by the PI controller. It is well known that with the increase of proportional coefficient of PI controllers, the response time is reduced, but, the control system becomes more prone to instability. On the other hand, in order to minimize the effect of PI controllers
phase lag on the compensation performance, the corner angular frequency of these controllers which can be calculated as the ratio of integral to proportional coefficients, should be set at one decade or more below the frequency of under compensation component [13]. Harmonic and unbalance variations are usually slow; thus, it is not necessary to apply high bandwidth PI controllers. Here, secondary level comprises PI controllers for compensation of SLB voltage fundamental negative sequence and 3rd, 5th and 7th harmonic components. The parameters of PI controllers are listed in Table III.

![Diagram of test system](image)

**Fig.4. Test system for simulation studies.**

**IV. SIMULATION RESULTS**

Fig.4 shows the simulation test system which is a two-DG islanded microgrid comprising two source buses, one sensitive load bus and one non-sensitive load bus. A diode rectifier and a star-connected linear load are connected to SLB. It is assumed that one phase of nonlinear load is disconnected to create unbalanced voltage distortion. Furthermore, a balanced nonlinear load is connected to NLB. Switching frequency of the DGs inverters is 10 kHz. The test system parameters are listed in Table I. Note that in this Table, the impedances of linear load and lines are presented in terms of resistance (ohm) and inductance (mH). Simulations are performed using MATLAB/Simulink.

Three simulation steps are considered:
- **Step 1** \( (0 \leq t < 2s) \)
  DGs operate only with fundamental positive sequence virtual impedance and secondary control is not acting.
- **Step 2** \( (2 \leq t < 4s) \)
  Virtual resistances for fundamental negative sequence and harmonic components are added.
- **Step 3** \( (4 \leq t < 7s) \)
  Secondary control is activated. The reference values of unbalance factor and harmonic distortion indices are 0.2%.
V. CONCLUSION:

A hierarchical control structure consisting of primary and secondary levels is proposed for microgrids. The secondary level controls selective compensation of SLB voltage fundamental negative sequence and positive and negative sequences of main harmonics by sending proper control signals to the primary level. A new method for sharing of harmonic compensation effort is presented. Moreover, a selective virtual impedance scheme is proposed to improve load sharing among the microgrid DGs. The control system design is discussed in detail. Simulation results show that the SLB voltage quality is enhanced significantly by using the proposed compensation method while the load current is shared properly.
VI. REFERENCES


